REMARKS

35 U.S.C. Section 101 Rejections

Applicants have here in further amended the specification to obviate the cited 35 USC section 101 rejection.

35 U.S.C. Section 103 Rejections

Paragraph 8 of the above referenced Office Action states that independent Claims 1, 11, and 21 are rejected under 35 USC section 103 as being rendered obvious by Devine (US Patent Number 6,397,242) in view of Patel (2004/0215444). Applicants have amended independent Claims 1, 11, and 21 to more particularly point out aspects of the present invention. Each of the independent claims have been amended to explicitly recite aspects regarding the micro architecture code with respect to the processor architecture hardware.

Each of the independent claims has been amended to explicitly recite aspects regarding the micro architecture code with respect to the processor architecture hardware. With respect to claim 1, Applicants have amended claim 1 to recite a method for supporting input/output for a virtual machine, comprising:

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executing virtual machine application instructions, wherein the application instructions are executed using micro architecture code of a

processor architecture, the micro architecture code configured to feed pipelines of the processor architecture hardware, wherein the micro architecture code includes an instruction interpreter to execute the virtual machine application instructions;

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As explicitly recited in claim 1, the micro architecture code of the processor architecture includes instruction interpreter to execute the virtual machine application instructions. The micro architecture code is specifically configured to feed pipelines of the processor architecture hardware. This micro architecture code is directly processed by the pipelines of the CPU. This is very different from, for example, Java byte code. Similar limitations are included in each of the independent claims 11 and 21.

Applicants have reviewed the Devine reference and assert that Devine does not show or suggest a micro architecture code instruction interpreter as in the claimed invention. Devine describes the operation of a virtual machine monitor, however, the detection of Devine (e.g., Devine col. 12 line 38) is not a micro architecture code instruction interpreter as in the claimed invention.

The above referenced office action relies upon Patel to show Java byte code interpreters as used by a Java virtual machine (e.g., Patel pp1 paragraph 0004, lines 7-8). Applicants point out that Java byte code is completely different than micro architecture instructions of an x86 processor. Java byte code cannot be directly operated upon by the internal hardware

(e.g., pipelines, etc.) of an x86 CPU. Java byte code, like other x86 instruction set code, is translated from x86 instructions into the internal micro architecture instructions that manipulate the hardware of the CPU.

Because of this, Applicant asserts that the present invention as recited in the amended Claims 1-30 is not rendered obvious by Devine in combination with Patel within the meaning of 35 USC Section 103.

With respect to dependent claims 2, 12 and 22, further limitations are recited, wherein the instruction interpreter is further configured to function with an instruction translator to translate target instructions into host VLIW instructions to execute the virtual machine application instructions. Applicant asserts that there is no disclosure or suggestion within Devine for any instruction translator operating in conjunction with an instruction interpreter to translate target instructions into host VLIW instructions.

With respect to dependent Claims 3, 13, and 23, further limitations are recited, wherein the micro architecture code includes an instruction translator to execute the virtual machine application instructions. There is no disclosure of translation (e.g., from a host instruction set to a target instruction set) to run both the virtual machine monitor and the virtual machine as in the claimed invention.

With respect to dependent Claims 8, 18 and 28, further limitations are recited, wherein the virtual machine application instructions comprise target instructions and the micro architecture code comprises host instructions. Applicants point out that the description of target instructions and host instructions are a particular result of the architecture of the processor of the claimed invention (e.g., utilizing an instruction interpreter and an instruction translator). Because of this, these limitation are not shown or suggested by the Devine and Patel references.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
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